IN THE SPECIFICATION:

Please replace the paragraph beginning at page 7, line 13, with the following rewritten paragraph:

[0015] The known circuit SC includes the first MISFET MNM1 forming a source-drain path between the storage node C of the static semiconductor memory SM and a ground potential (GND) and the second MISFET [[MNM 1]] MNM2 forming a source-drain path between the storage node C_ and the ground potential (GND). Gate terminals of the first and second MISFETs MNM1 and MNM2 connect to a word line WLW.

Please replace the paragraph beginning at page 8, line 1, with the following rewritten paragraph:

[0017] With this configuration, the storage circuit shown in Fig. 12 functions as a static semiconductor memory (SRAM) if a RESTORE signal is at a power supply potential, if a WLW signal is at a ground potential, and if an EQ signal is at the power supply potential. On the other hand, the storage circuit shown in Fig. 12 functions as a semiconductor nonvolatile storage circuit equivalent to the known circuit shown in Fig. 7 if the ~~STORE~~ RESTORE signal is at the ground potential, if the WLW signal is at the power supply potential, and if the EQ signal is at the ground potential

Please replace the paragraph beginning at page 39, line 4, with the following rewritten paragraph:

[0039] The third MISFET MNM3 forms a source-drain path between the drain terminal of the first MISFET MNM1 and the bit line BL, and the fourth MISFET MNM4 forms a source-drain path between the drain terminal of the second MISFET MNM2 and the differential pair line BL_. Gate terminals of the third and fourth MISFETs MNM3 and MNM4 connect to a word line WLS. The third and fourth MISFETs [[MNM5]] MNM3 and [[MNM6]] MNM4 are n-type MISFETs.

Please replace the paragraph beginning at page 20, line 17, with the following rewritten paragraph:

[0046] Fig. 6 is a circuit diagram showing a storage circuit according to a fourth embodiment of the present invention. This storage circuit is formed by connecting the two storage nodes of the known static semiconductor memory SM to input and output terminals of a semiconductor nonvolatile storage circuit SI. The static semiconductor memory SM has the same configuration as that of the circuit shown in Fig. [[11]] 12. The elements thereof are denoted by the same reference numerals and thus the corresponding description is omitted.

Please replace the paragraph beginning at page 21, line 1, with the following rewritten paragraph:

[0047] In the semiconductor nonvolatile storage circuit SI, as in the semiconductor nonvolatile storage circuit according to the first embodiment, the source terminals of the first and second MISFETs MNM1 and MNM2 connect to the ground potential GND, the gate terminals thereof connect to a word line WLW, the drain terminal of the first MISFET MNM1 connects to the source terminal of the third MISFET MNM3, the drain terminal of the third MISFET MNM3 connects to a storage node C of the static semiconductor memory SM, the drain terminal of the second MISFET MNM2 connects to the source terminal of the fourth MISFET MNM4, the drain terminal of the fourth MISFET [[MNM3]] MNM4 connects to a storage node C_ of the static semiconductor memory SM, and the gate terminals of the third and fourth MISFETs MNM3 and MNM4 connect to a word line WLWS. As in the first embodiment, a WLWS signal is risen or fallen in synchronization with a WLW signal.

Please replace the paragraph beginning at page 21, line 18, and bridging to page 22, line 3, with the following rewritten paragraph:

[0048] With this configuration, this circuit functions as a static semiconductor memory if a RESTORE signal is set to the power supply potential, if a WLW signal is set to the ground potential GND, and if an EQ signal is set to the power supply potential VDD. On the other hand, this circuit functions as a circuit equivalent to the semiconductor nonvolatile storage circuit according to the

first embodiment if the ~~STORE~~ RESTORE signal is set to the ground potential GND, if the WLW signal is set to the power supply potential VDD, and if the EQ signal is set to the ground potential GND.